AD-A048 307 TEXAS INSTRUMENTS INC DALLAS F/G 13/8
IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY.(U)
JUL 77 G L VARNELL, R A WILLIAMSON DAAB07-76-C-8105
UNCLASSIFIED TI-03-77-30 NL

1 OF 1
ADA048307

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Report No. 03-77-30

Second Quarterly Report

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Period Covered
1 December 1976 – 1 March 1977

Contract No. DAAB07-76-C-8105

Procurement and Production Directorate
U.S. Army Electronics Command
Fort Monmouth, New Jersey 07703

Texas Instruments Incorporated
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Dallas, Texas 75222

ACKNOWLEDGMENT

This project has been accomplished as part of the U.S. Army Manufacturing and Technology Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to ensure the efficient production of current or future defense programs.

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Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE *(and Subtitle)*

(6) IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY,

(9) 5. ~~TYPE OF REPORT & PERIOD COVERED~~

Quarterly rept. no. 2,
1 Dec [redacted]76 – 1 Mar [redacted]77,

6. PERFORMING ORG. REPORT NUMBER

(14) TI – 03-77-30

7. AUTHOR(s)

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8. CONTRACT OR GRANT NUMBER(s)

(15) DAAB07-76-C-8105

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Texas Instruments, Inc.
P.O. Box 5012
Dallas, Texas 75222

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

276 9631

11. CONTROLLING OFFICE NAME AND ADDRESS

Procurement & Production Directorate
U.S. Army Electronics Command
Fort Monmouth, New Jersey

(11) 12. REPORT DATE

July [redacted]977

13. NUMBER OF PAGES

31

14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*

(12) 36p.

15. SECURITY CLASS. *(of this report)*

Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

electron beam
e-beam resists
256 Bit Bipolar AM

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The technical and economic impact of electron-beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. All electron-beam tapes necessary for fabricating the 256-bit bipolar RAMs have been generated. Advanced software techniques such as geometry sizing, sorting and increment/decrement were used. E-beam processes have been developed for all lithographic steps on the 256-bit bipolar RAMs. Because of the pattern distortion at

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DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

347 650

ABSTRACT (Continued)

epitaxial growth, the original alignment marker system was modified. Several lots using this new alignment marker system are in process. The design of the Automatic Slice Loader is complete.

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Second Quarterly Report

1 December 1976 – 1 March 1977

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SECTION I
PURPOSE

The overall objective of the program is to implement e-beam writing technology for the fabrication of microcircuits. The technical and economic impact of electron beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. The elimination of mask masters, masks, and the masking process will eliminate the most significant source of yield loss. This will permit greater circuit design complexity and flexibility which will lead to lower device costs with increased reliability. The complete implementation program is divided into three tasks. Task A, Yield Improvement Through Direct E-Beam Writing, is directed toward developing the manufacturing technology required for e-beam writing with existing equipment and existing resist processes and demonstrating the yield benefits of this technique. Task B, Cost Reduction for E-beam Writing Through High Speed Resist Implementation, is directed toward implementing identified high speed e-beam resists in order to significantly decrease cycle time and thus reduce the IC bar cost. Task C, Cost Reduction for E-Beam Writing Through Automatic Beam Diameter Control and Automatic Handling, is directed toward utilizing EBMIII's capability of computer-controlled beam size (large and small) on high density circuit ($\leq$0.1 mil) geometries. This program also included implementation of an automated handling system for slices to reduce cycle time and thus further reduce bar cost.

SECTION II
NARRATIVE AND DATA

A. SCHOTTKY BIPOLAR RAM PROCESSING

1. Introduction

There are many possible bipolar processes that could be used in conjunction with e-beam pattern definition to build memory devices. Among those are dielectric isolation, isoplanar, etc. While all of these processes have merit, the process chosen for this program will be the junction isolation double-level metal Schottky process which is used by Texas Instruments in building the 54S/74S series of RAMs.

2. Process Description

The process to be used is outlined in Table I and Figure 1. Some procedures such as clean-ups and etches are omitted from the table but of course are used and are typical of good production practice.

Table I. Schottky Bipolar RAM Process

1)	Substrate	14)	Base drive
2)	Initial Oxidation	15)	Emitter oxide removal
3)	DUF oxide removal	16)	Emitter deposition and drive
4)	DUF deposition	17)	Contact oxide removal
5)	DUF drive	18)	Platinum deposition
6)	Strip oxide	19)	Alloy platinum
7)	Epitaxial layer	20)	Ti-W, Aluminum deposition
8)	Second oxidation	21)	Metal removal I
9)	Isolation oxide removal	22)	Dielectric deposition
10)	Isolation deposition	23)	Vias
11)	Isolation drive	24)	Aluminum deposition
12)	Base oxide removal	25)	Metal removal II
13)	Base deposition	26)	Sinter metal

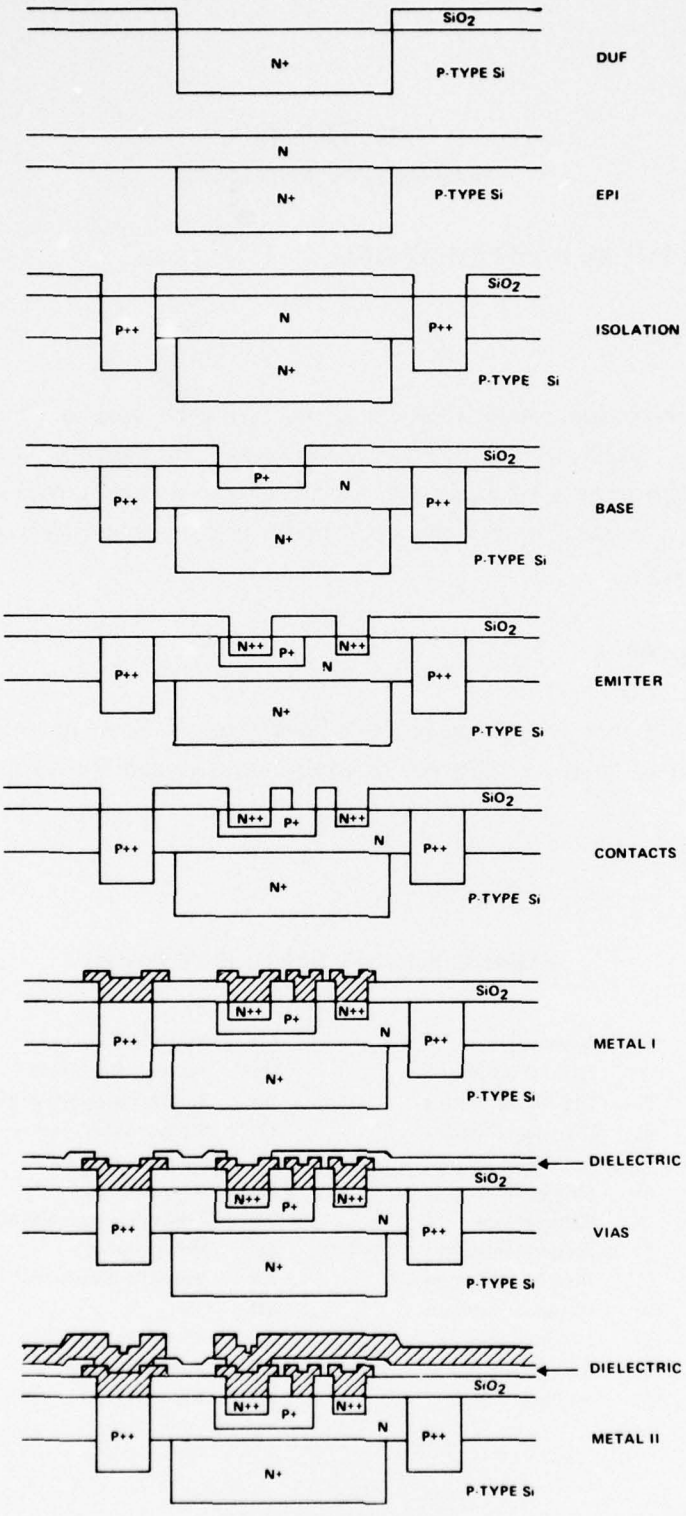

Figure 1. Sectional View of Slice at Various Steps

3. Resist and Etch Selection

Except for metallization, the patterning steps shown above involve etching between 2000 Å and 10,000 Å of SiO_2. Because plasma etch rates of SiO_2 are low and resist lifetimes are limited in the plasma environment, we intend to etch SiO_2 using common buffered HF solutions. Our requirements for electron resists are thus dominated by two factors: 1) high speed ($\geq 2.5\ \mu C/cm^2$) and 2) good adhesion to SiO_2 for wet chemical etching. Among the resists that we have investigated whose sensitivities are greater than $2.5\ \mu C/cm^2$, we have demonstrated good oxide patterning capability with polybutene sulfone (PBS) resist. Further, PBS, being a positive resist, leads to advantages in minimizing area scanned and increasing throughput for most of the pattern levels.

Metallization for the 256-bit RAM will be two levels of metal separated by a dielectric. The first level will be Ti-W/Al and the second level will be pure Al.

PBS cannot be used as a plasma etch mask and there are no other high-speed positive resists available. We will therefore use the negative resist TI309, which has a sensitivity of $\approx 2.5\ \mu C/cm^2$. Some experimental results have been completed which show that Al can be plasma etched using TI309 as a mask; however, we will not attempt to etch the first level of metallization using a plasma. Plasma etching gives very steep steps in the etched material and would make second level metal coverage impossible. Any attempts at plasma etching aluminum will be restricted to the second level of metallization. If difficulty arises in trying to plasma etch the second level of metallization, the wet chemical etchants, which will be used on the first metallization level, can be substituted.

Resist processing will be done on completely automated, cassette loaded spin coaters and developers. This will provide maximum throughput and reproducibility while minimizing slice handling. These machines are installed in a horizontal laminar flow clean room to minimize particulate contamination. Wet chemical processing will be performed in vertical laminar flow clean hoods installed in this same room.

The feasibility of IR baking for electron resist processing will be demonstrated. Cassette loaded ovens with belt drive through three temperature zones and nitrogen air curtains will be used. The wafers will load individually onto the belt and face the IR emitters directly.

B. SCHOTTKY BIPOLAR RAM DESIGN

1. Inputs

The circuit schematic for all of the inputs is shown in Figure 2. This circuitry was designed to give very low high- and low-level input currents and very high performance. The low input currents allow higher fan-out capability in an entire memory system. The use of Schottky diodes and transistors in the inputs increases the performance over non-Schottky devices. The inputs also have clamp diodes to protect the circuitry if the input voltage should go negative.

2. Output

The circuit schematic for the output is shown in Figure 3. The open-collector output permits connection of one, or for larger word capacities, a number of outputs to a common bus through a single pull-up termination.

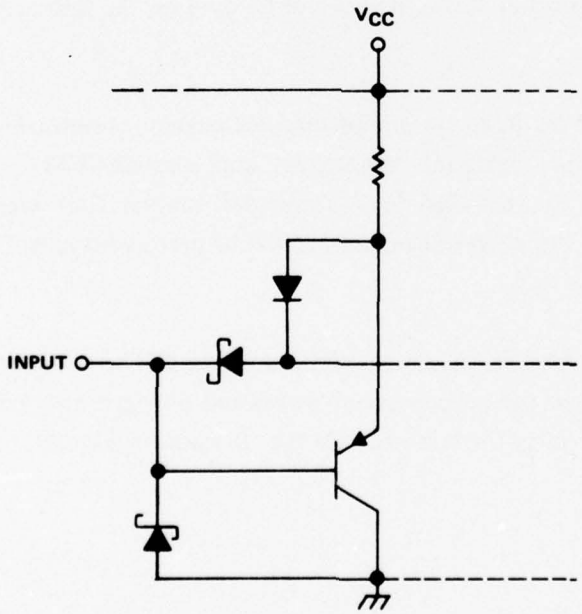

Figure 2. Input Circuitry

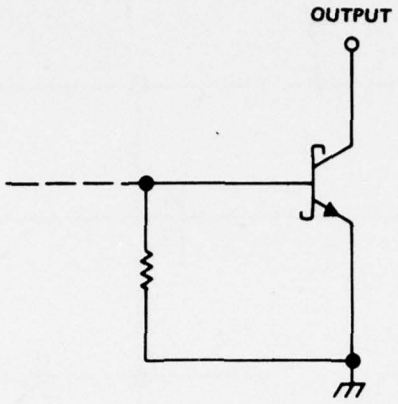

Figure 3. Output Circuitry

3. Memory Cell

The circuit schematic for the memory cell is shown in Figure 4. The cell is basically two cross-coupled inverters and two sense diodes. Information is written into the cell or read from the cell along the sense lines. The cell is enabled or disabled using the word line. When the word line is low, information can be read from or written into the cell. When the word line is in a high state the cell is disabled and no information can be read or written.

4. System Design

The IC is a single monolithic integrated circuit containing a 256-word by 1-bit fully static random access non-destructive readout memory. The memory if fully decoded requires only 8 address lines to select one of 256 storage locations. An additional line, write enable, is provided to enable the memory to modify the stored data. Separate Data Input and Data Output lines are provided for minimum interaction between input and output functions. Three chip enable lines are provided to simplify the decoding required to achieve the desired system.

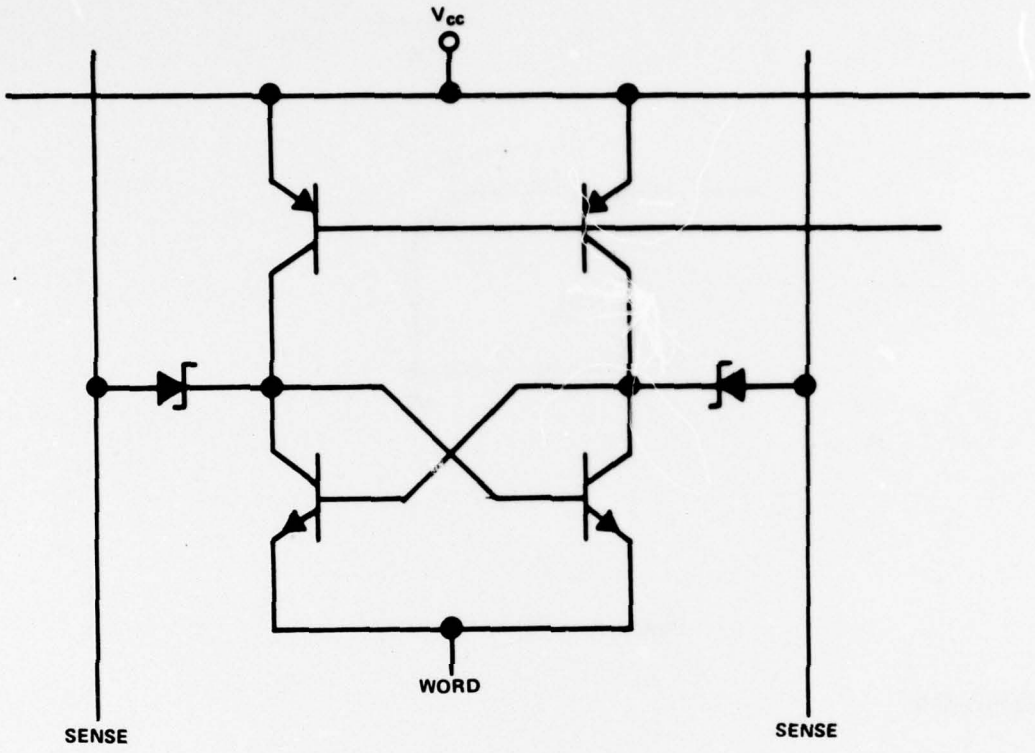

Figure 4. Memory Cell

The basic logic diagram is shown in Figure 5. The memory matrix is organized in an array of 16 rows and 16 columns. The address inputs A, B, C and H go to a 4-to-16 line decoder and determine the memory column selected. The address inputs D, E, F and G go to a 4-to-16 line decoder and determine the memory row selected. The logical operational mode (truth table) is shown in Table II.

5. Terminal Connections

The terminal connections for the 256-bit RAM are shown in Figure 6.

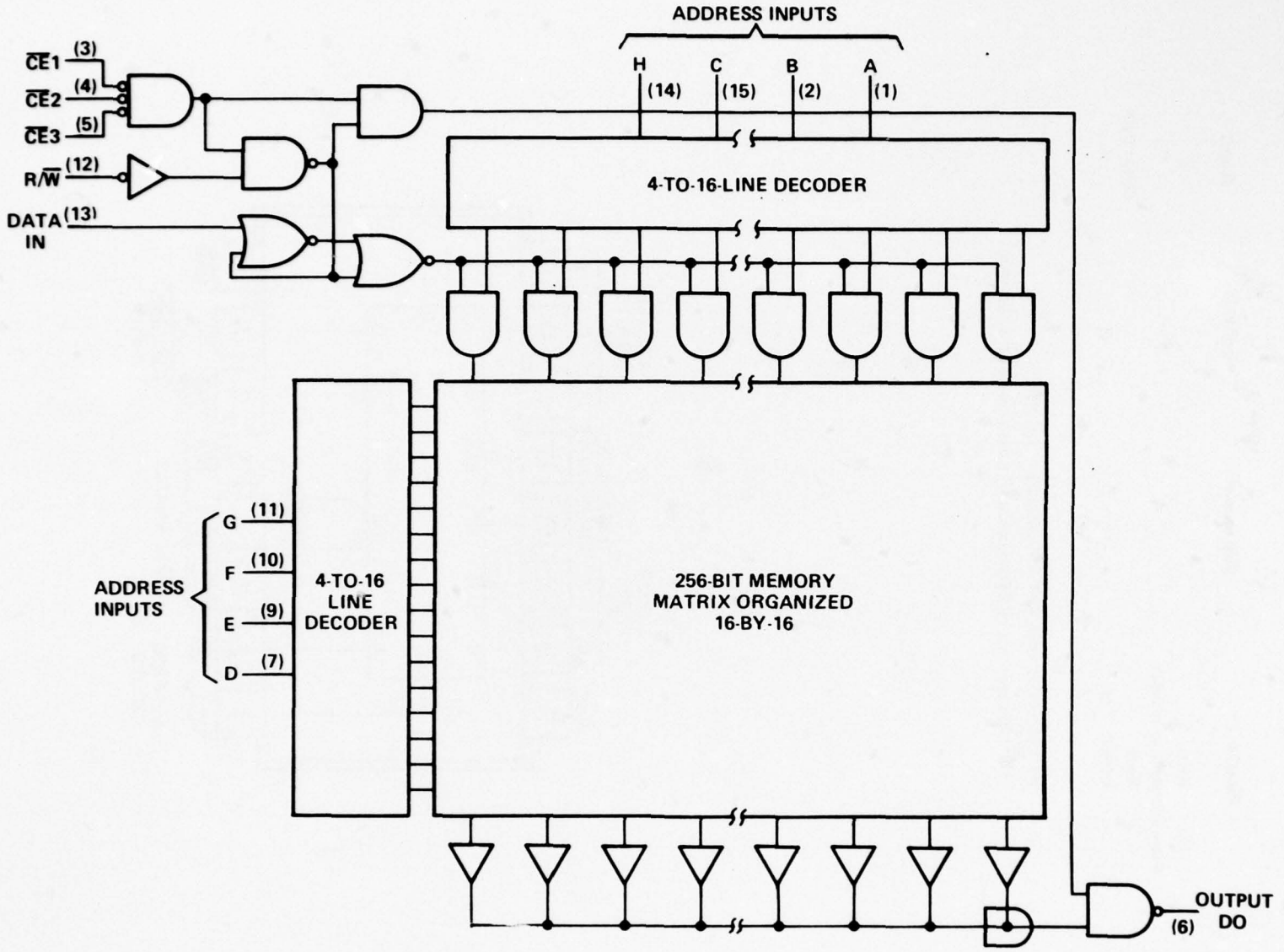

Figure 5. Logic Diagram

Table II. Logical Operational Mode

Function	Inputs: Chip Enable†	Inputs: Read/Write	Output
Write (Store Complement of Data)	L	L	H
Read	L	L	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For chip-enable: L = all $\overline{CE}$ inputs low; H = one or more $\overline{CE}$ inputs High

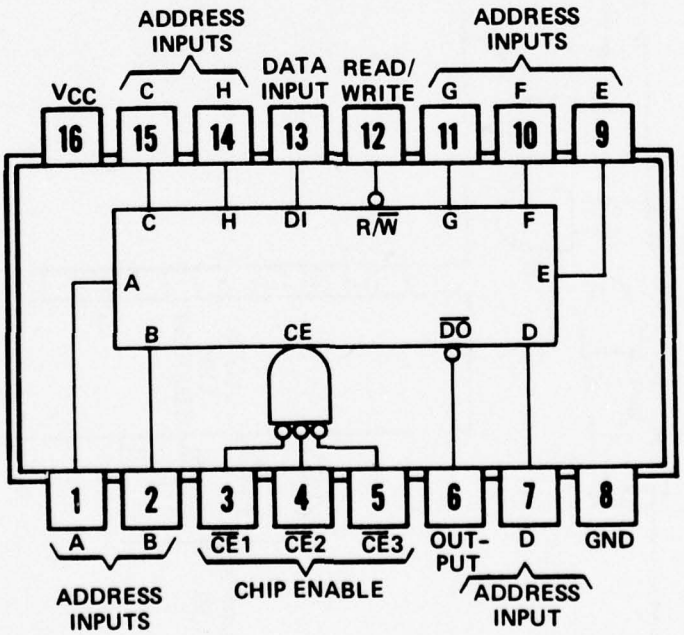

Figure 6. Terminal Connections

C. ELECTRICAL TESTING

Electrical testing for the 256-bit RAM will be accomplished using existing automatic test systems at Texas Instruments. The basic equipment proposed for the test is the High Speed Measurement (HSM) System and the Numerical Exerciser for Memories (NEM).

The HSM will be used to test the memories while they are in slice form. It will perform all the dc tests such as I_{CC}, V_{OL}, I_{OH}, etc. and will also do functional testing on the memory cells and peripheral circuitry.

The NEM will be used to test the memories after they have been packaged. Programming of the NEM is accomplished with a RAM memory supplying instructions for support as well as test instructions to implement exercise algorithms. Some of the algorithms presently in the software library are as follows:

1) (a) Write a zero in each device location (1, 2, 3 . . . N)

   (b) Read and verify a zero in each location (1, 2, 3 . . . N)

   (c) Write a one in each device location (1, 2, 3 . . . N)

   (d) Read and verify a one in each location (1, 2, 3 . . . N)

2) (a) Read a one in first cell, write back a zero, and read a zero. Repeat process for all cells (1, 2, 3 . . . N)

   (b) Read a zero in the first cell, write back a one; and read a one. Repeat process for all cells (1, 2, 3 . . . N)

   (c) Repeat (a) backwards – last cell first. (N, N-1, N-2 . . . 1)

   (d) Repeat (b) backwards – last cell first. (N, N-1, N-2 . . . 1)

3) Access 0-1-0: This algorithm starts with a memory full of zeros and a 1 in location 0. Begin by reading a background of "0", a reference location of "1" and again reading a background of "0". Repeating this process, thus, verifies the access time (address to data output) "both ways" between location 0 and all other locations, 1 through N: then writes a one into location 1 and verifies its access time with respect to all remaining locations 2 through N; then reiterates this process until a one is written into the final location N, whose accesss times with respect to all other locations have already been verified. Notice that data out complements for both directions of read access.

4) Access 1-0-1: This test initializes the device to all ones, then tests individual access times by using the same general procedures as in test 3 above except that all data zero/one references are reversed. This time the data output transitions for each read cycle are 1-0-1.

5) Random data pattern: This test will generate a 10 bit MLS pseudo random data sequence for writing into and reading from the device under test. The sequence repeats after 1023 memory cycles. This pattern will be displayed by one bit prior to each write all, read all such that after n loops, the random pattern will have been rotated completely through memory.

6) Walking Disturb: This is the most thorough single test of all present algorithms. It is a combination of the "walking ones and zeros", access time verify to and from every location and, address to write enable set-up check to and from every memory address. With the exception of memory enable/exercise, it will do an equal to or better than evaluation of any failure mode exercised by all the preceding algorithms. However, it does have a limitation; execution time.

The NEM system is designed such that generating new algorithms is almost limited to one's own imagination.

All of the final functional dc and ac testing will be performed on the NEM. The memories will be tested according to specification SCS-517 (2/12/76) and will meet all electrical requirements of that specification.

SECTION III
RESULTS

A. E-BEAM TAPES

1. Introduction

Pattern descriptions are accepted in two formats on EBMIIIA: Pattern Definition Language (PDL) and Electron Beam Magnetic Tape. PDL is normally used for small amounts of data (test bars, exposure, patterns, etc.). The 256-bit bipolar RAM patterns are input on e-beam magnetic tapes. The input figures are rectangles with sides parallel to the axes and trapezoids with the sides parallel to the axes. The patterns are decomposed into these figures by algorithms on the IBM 370 computer. In order to achieve the proper geometry line widths in PBS electron resist, it is necessary to undersize all geometries before exposure. The previous composition algorithms did not allow undersizing. An internal software development program has been underway during the last year to allow undersizing of all geometries. This was successfully completed in February 1977 so that it is now a simple matter to undersize all geometries and compensate for the exposure characteristics of PBS. This has been the major factor in delaying processing of the 256-bit bipolar RAM slices.

In addition, the new interface on EBMIII was designed to generate geometries no larger than 1/16 X 1/16 of the field size. Since frequency related errors and pattern generation length errors are proportional to the line lengths, these errors are reduced by 16X over the previous interface design. The software required to decompose geometries larger than 1/16 X 1/16 of the field size has been implemented.

2. Tape Status

All of the e-beam tapes for the 256-bit RAM have been processed and received. They have been loaded on EBMIII and checked by exposing the patterns on blank slices. Pictures of these exposures are shown in Figures 7-19.

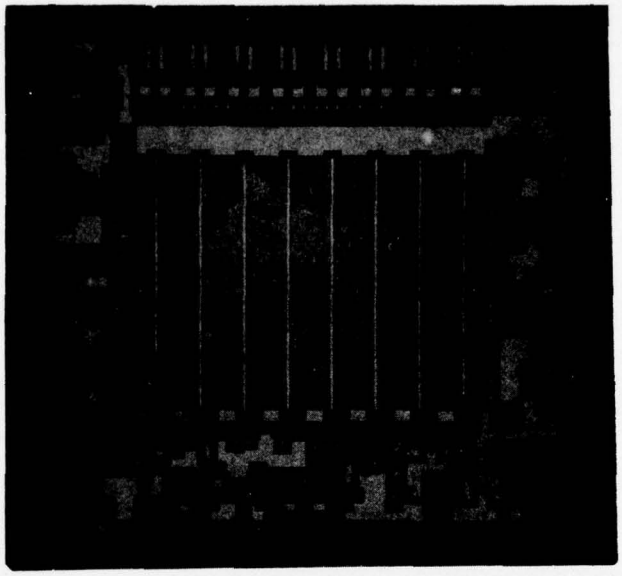

Figure 7. DUF Pattern Exposed in Resist

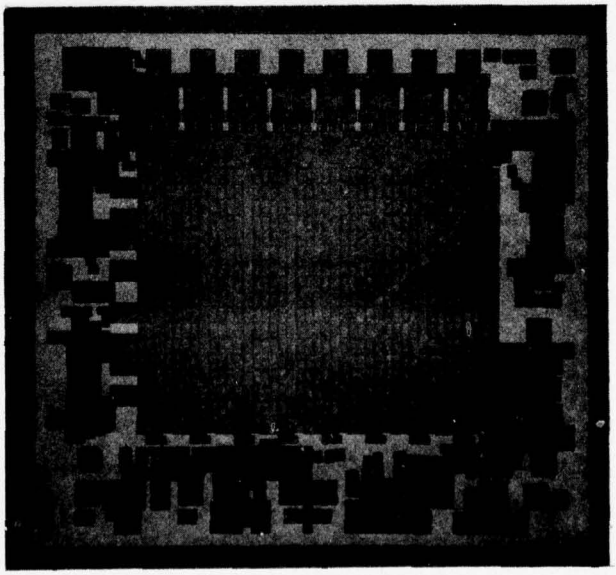

Figure 8. Isolation Pattern Exposed in Resist

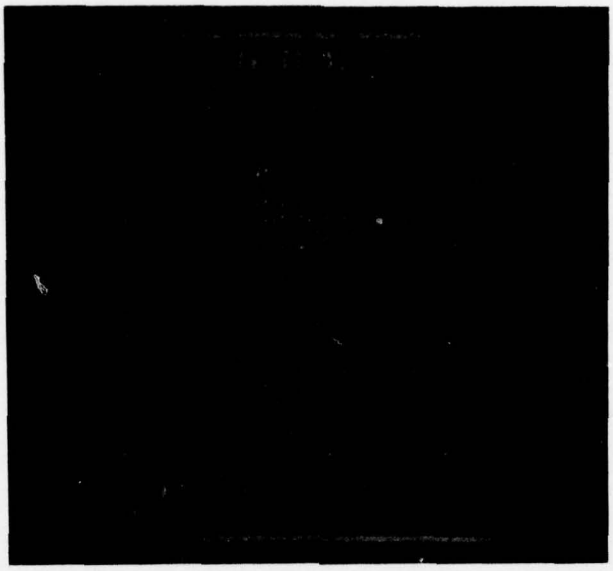

Figure 9. Base Pattern Exposed in Resist

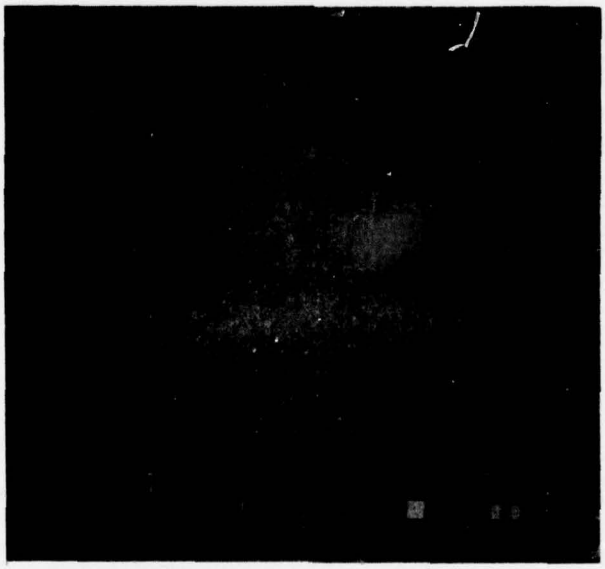

Figure 10. Emitter Pattern Exposed in Resist

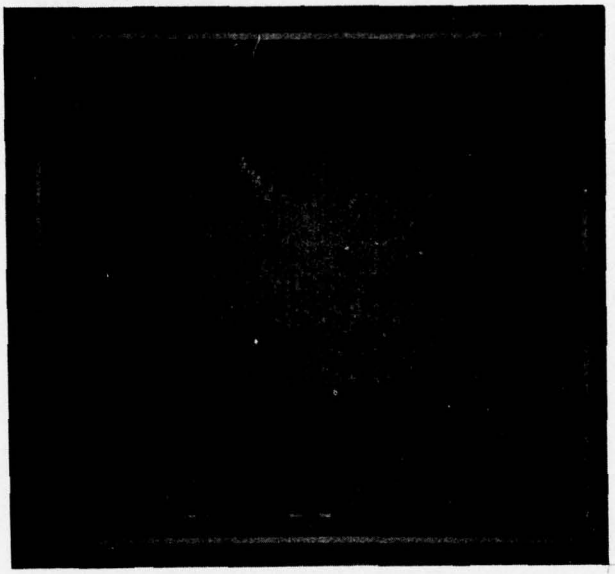

Figure 11. Contact Pattern Exposed in Resist

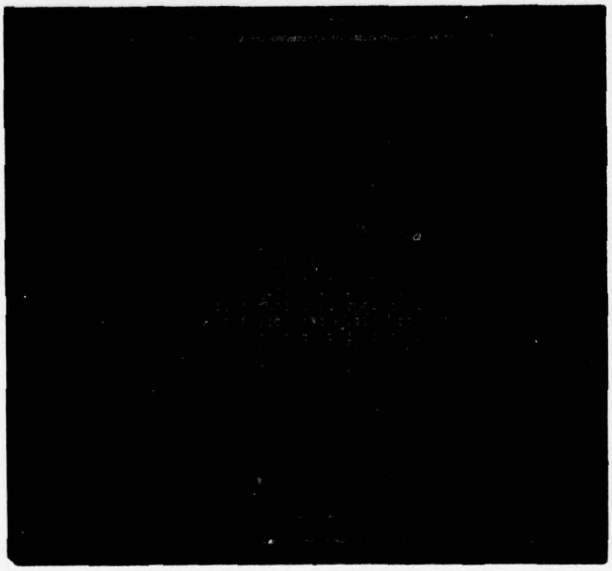

Figure 12. P-Contacts

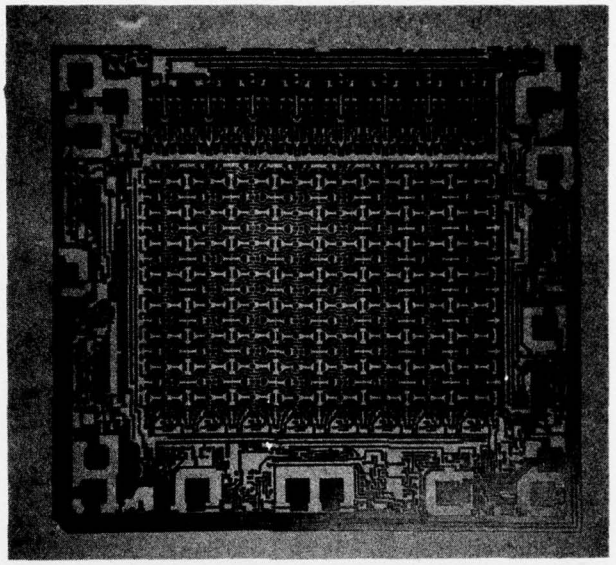

Figure 13. Leads I Pattern Exposed in Resist

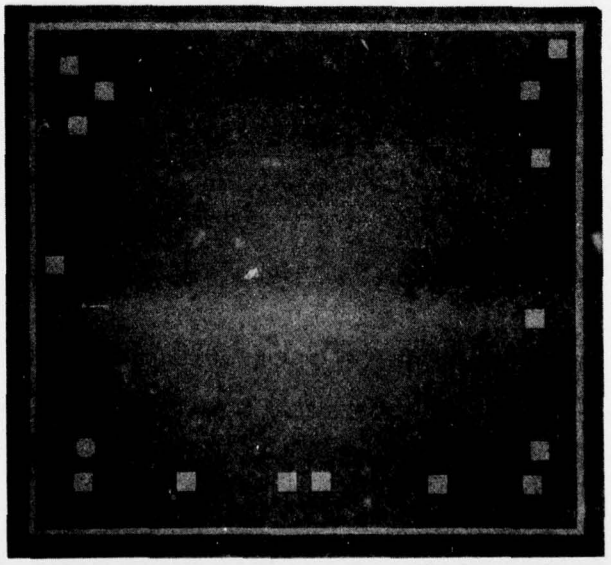

Figure 14. Vias Pattern Exposed in Resist

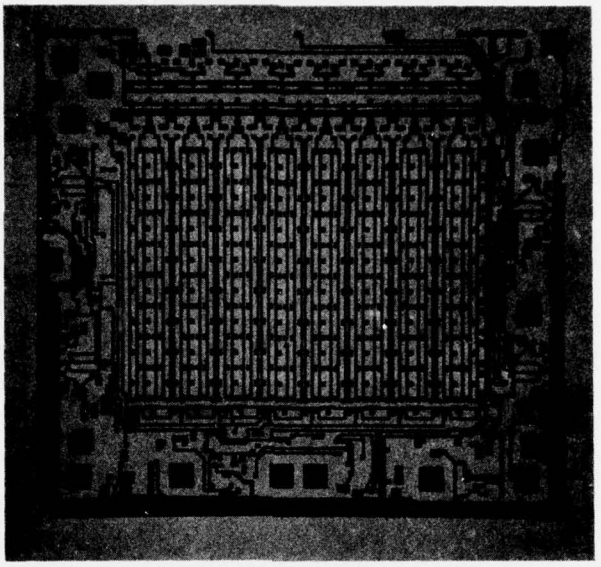

Figure 15. Leads II Pattern Exposed in Resist

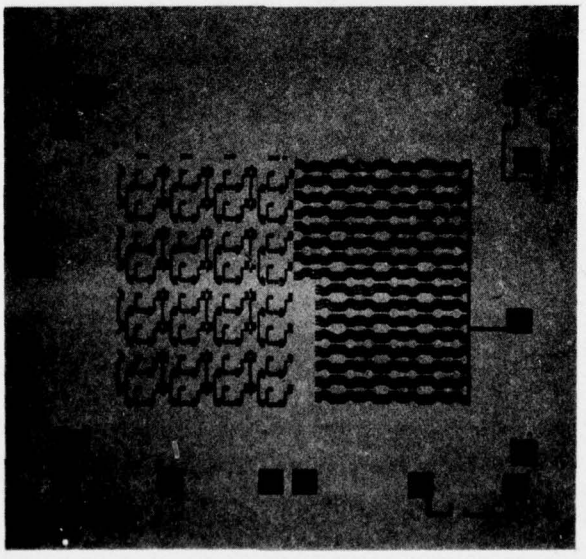

Figure 16. Test Leads 1A Pattern Exposed in Resist

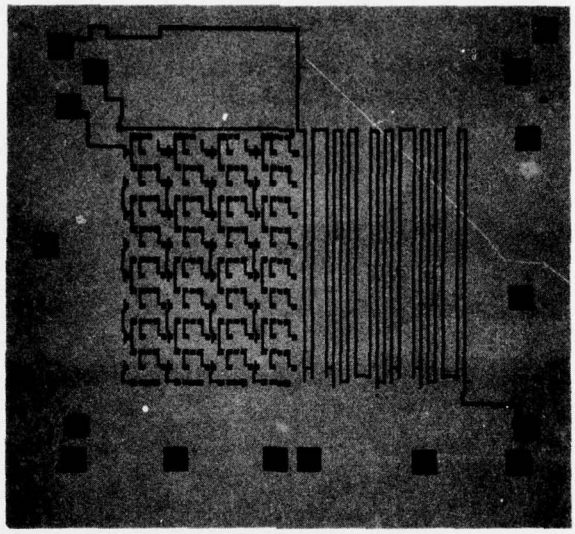

Figure 17. Test Leads 2A Pattern Exposed in Resist

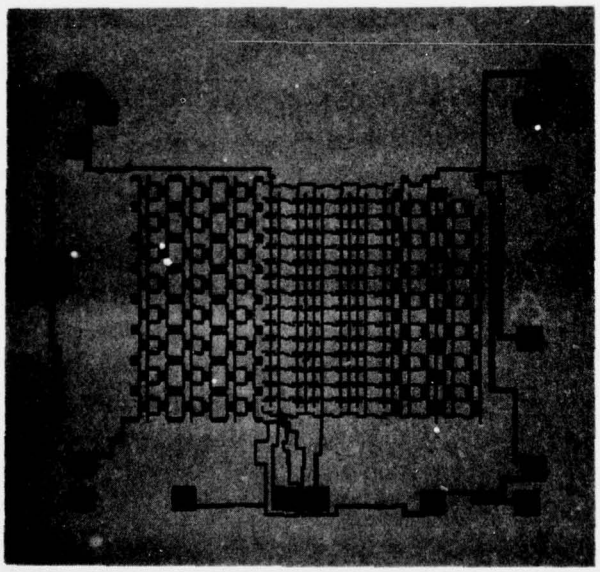

Figure 18. Test Leads 1B Pattern Exposed in Resist

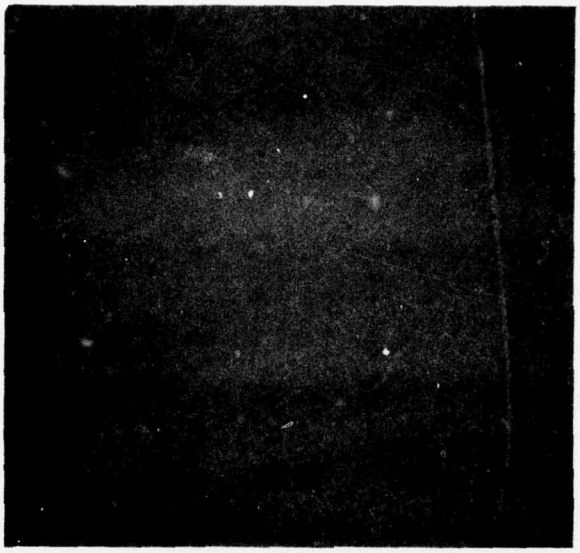

Figure 19. Test Leads 2B Pattern Exposed in Resist

B. SLICE PROCESSING

1. General Discussion

Table III lists the process step, resist and etch process for each level in the fabrication process. The actual specifics of each lithographic step, such as spin speeds, bake temperatures, etc., are listed below. Only the alignment marker and DUF O.R. processes have been used on the material in process because that is as far as the slices have progressed. However, the processes have been verified on test slices and they will by used when the material reaches those process steps.

Table III. Process Step, Resist, and Etch Process for Fabrication Level

Process Step	Resist	Etch Process
Alignment Markers I and II	PMMA	Plasma
DUF	PBS	Buffered HF
Isolation	PBS	Buffered HF
Base	PBS	Buffered HF
Emitter	PBS	Buffered HF
Contact	PBS	Buffered HF
Leads I	TI resist No. 309	Metex Etch
Vias	PBS	Ethylene Glycol/HF
Leads II	TI resist No. 309	Metex Etch

2. E-Beam Lithographic Process

Alignment Markers I and II Steps

1. Bake – IR @ 160°C
2. Coat – 8% PMMA @ 1.5K RPM
3. Bake – IR @ 160°C
4. Expose
5. Develop – Methyl Isobutylketone/Isopropyl Alcohol
6. Bake – IR @ 160°C
7. Plasma De-scum – O_2 @ 100 watts
8. Plasma etch – CF_4/O_2 @ 300 watts
9. Clean-up – Plasma, 10 min O_2 @ 300 watts

DUF and Isolation Steps

1. Coat – 8% PMMA @ 1.5K RPM
2. Bake – IR @ 160°C
3. Coat – 8% PMMA @ 1.5K RPM
4. Bake – IR @ 160°C
5. Etch – Buffered HF until back side clears
6. Rinse and Spin Rinse/Dry
7. Clean-up – Asher, 15 min O_2 @ 300 watts
8. Steam slices – 5 min @ 700°C
9. Coat – 5% PBS @ 2K RPM
10. Bake – IR @ 120°C
11. Expose
12. Develop – PBS Developer
13. Bake – IR @ 120°C

14. Etch – Buffered HF
15. Rinse and Spin Rinse/Dry
16. Clean-up – Methyl Ethyl Ketone Strip, IPA rinse, D.I. H_2O, Spin Rinse/Dry

Base and Emitter Steps

1. Steam Slices – 5 min @ 700°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C
4. Etch – Buffered HF until back side clears
5. Rinse and Spin Rinse/Dry
6. Bake – IR @ 120°C
7. Expose
8. Develop – PBS Developer
9. Bake – IR @ 120°C
10. Etch – Buffered HF
11. Rinse and Spin Rinse/Dry
12. Clean-up – Methyl Ethyl Ketone Strip, IPA Rinse, D.I. H_2O, Spin Rinse/Dry

Contact Steps

1. N_2 bake slices – 30 min @ 700°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C
4. Expose – P-Contacts and Schottky
5. Develop – PBS Developer
6. Bake – IR @ 120°C
7. Etch – Buffered HF
8. Rinse – D.I. H_2O

9. Dry – N_2 Box
10. Bake – IR @ 120°C
11. Expose – N-Contacts
12. Develop – PBS Developer
13. Bake – IR @ 120°C
14. Etch – Buffered HF
15. Rinse and Spin Rinse/Dry
16. Clean-up – Methyl Ethyl Ketone Strip, IPA rinse, D.I. H_2O, Spin Rinse/Dry

Leads I Step

1. Bake – IR @ 160°C
2. Coat – TI309 @ 3K RPM
3. Bake – 50°C Air
4. Expose
5. Develop – Xylene/IPA
6. Bake – IR @ 160°C
7. Plasma De-scum – 2 min O_2 @ 100 watts
8. Etch – Metex Etch
9. Rinse and Spin Rinse/Dry
10. Bake – IR @ 120°C
11. Etch – Hydrogen Peroxide @ 30°C
12. Rinse and Spin Rinse/Dry
13. Clean-up – Plasma, 10 min O_2 @ 300 watts

Vias Step

1. Bake – IR @ 160°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C

4. Expose
5. Develop – PBS Developer
6. Bake – IR @ 120°C
7. Etch – Ethylene Glycol/HF
8. Rinse and Spin Rinse/Dry
9. Clean-up – Methyl Ethyl Ketone Strip, IPA Rinse, D.I. H_2O, Spin Rinse/Dry

Leads II Step

1. Bake – IR @ 160°C
2. Coat – TI309 @ 3K RPM
3. Bake – 50°C Air
4. Expose
5. Develop – Xylene/IPA
6. Bake – IR @ 160°C
7. Plasma De-scum – 2 min O_2 @ 100 watts
8. Etch – Metex Etch
9. Rinse and Spin Rinse/Dry
10. Clean-up – Plasma, 10 min O_2 @ 100 watts

3. Alignment Markers

The alignment markers have been fabricated by plasma etching bare silicon slices patterned with PMMA. E-beam alignment markers are featured 2 to 4 μm deep in the silicon substrate. This step has proceeded immediately subsequent to receiving the polished substrates. This procedure yields markers that are alignable at this point in the process. However, after these slices have been through the epitaxial layer growth step, the markers are no longer adequate for automatic alignment at the accuracies necessary to meet design tolerances of the chip. Pictures of a marker before and after the epitaxial process are shown in Figures 20 and 21, respectively. SEMs of the cross section of the marker are shown in Figures 22 and 23 clearly indicating why this particular marker was unsatisfactory for aligning after it had been through the epitaxial process. One edge of the marker had been completely etched away during vapor etching prior to epitaxial growth.

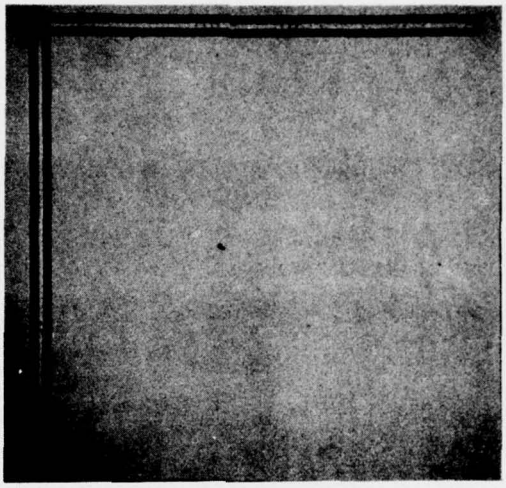

Figure 20. Plasma Etched Alignment Marker Before Epi

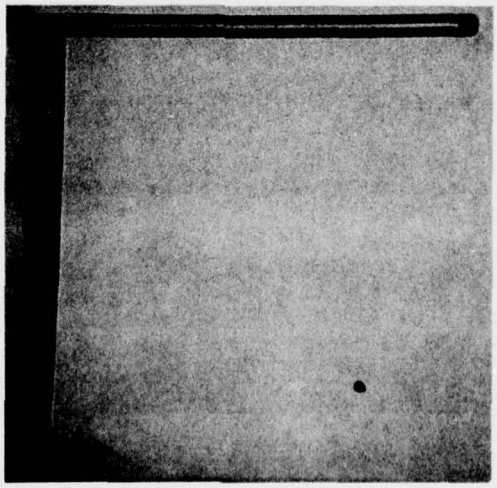

Figure 21. Plasma Etched Alignment Marker After Epi

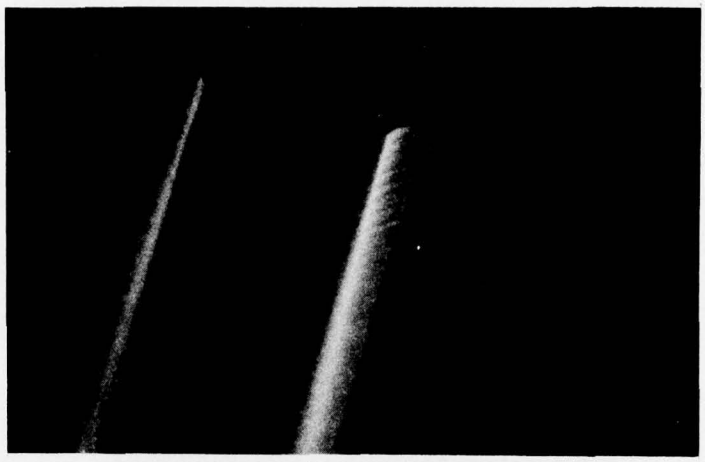

Figure 22. SEM of Plasma Etched Alignment Marker Before Epi

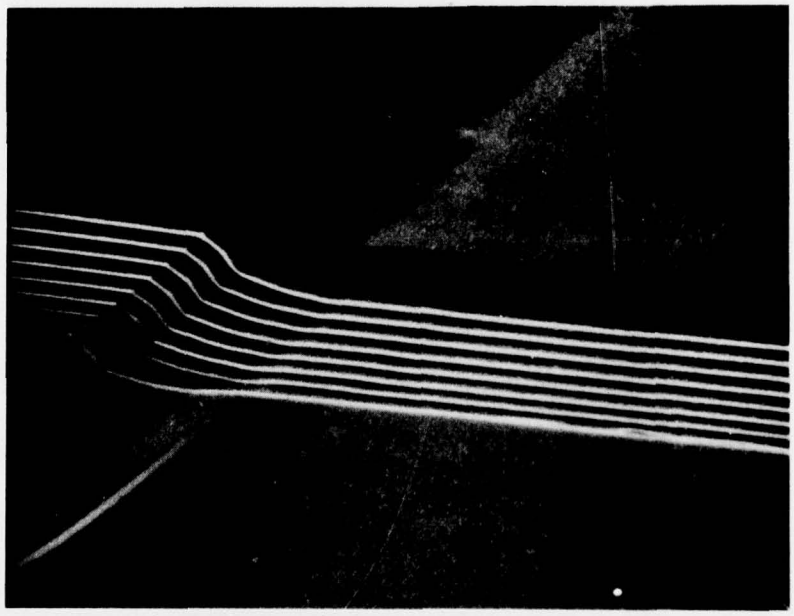

Figure 23. SEM of Plasma Etched Alignment Marker After Epi

The temporary solution to this problem has been to go to two sets of alignment markers, one fabricated at the same stage of the process as the original markers and the other fabricated immediately after the epitaxial step. The second set of markers is automatically aligned to the first set using loose alignment tolerances. The offset and gain errors introduced by using these looser tolerances are then measured and corrections are made such that all subsequent levels are placed correctly. Note that all levels placed after the second set of markers are aligned to the second set of markers. Figures 24 and 25 show the slice placement of the two sets of markers. Table IV shows a brief process comparison between the one marker set and two marker set systems.

4. Back Side Strip

As noted in the by-level listing of the processes, prior to each O.R. step (except contact), the oxide is removed from the back side of the slices. This is done to prevent the slices from charging up and deflecting the incident electron beam. Of course if the beam is deflected, the pattern is displaced. The slice back side is not stripped at contact O.R. because experimental results indicate it is unnecessary, probably because of the thin oxide on the back side.

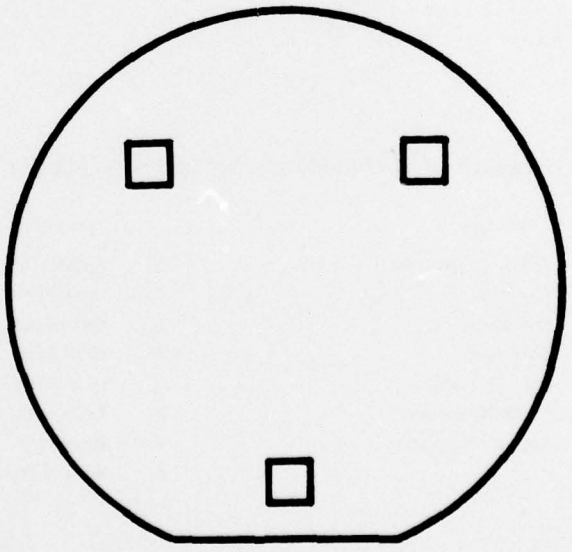

Figure 24. Placement of Markers I

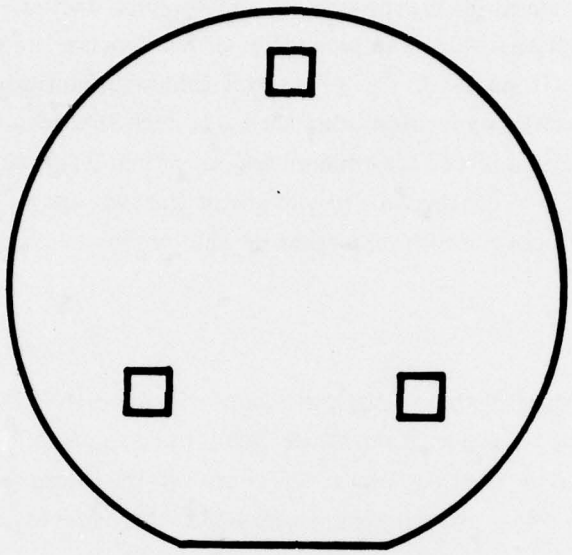

Figure 25. Placement of Markers II

Table IV. Comparison of One Marker Set and Two Marker Set Systems

	One Set		Two Sets
1.	Polished Substrate	1.	Polished Substrate
2.	Markers	2.	Markers I
3.	Oxidation	3.	Oxidation
4.	DUF O.R.	4.	DUF O.R.
5.	DUF Diffusion	5.	DUF Diffusion
6.	Epitaxial Growth	6.	Epitaxial Growth
7.	Second Oxidation	7.	Markers II
		8.	Second Oxidation

5. Pattern Exposure

The normal procedure when exposing a slice is to expose a chip, move to the next chip, expose, etc. This procedure is not the most efficient in terms of total slice exposure time since there is a stepping time associated with each chip exposure time. The method we are using exposes a 2 X 2 array of chips for every stepping time, thereby reducing by 75% the stepping time of the slice. This time reduction is significant since there are approximately 500 chips per slice.

6. Status

Three lots of material are presently in progress. All three will use the dual alignment marker system discussed previously.

SECTION IV
MANPOWER

The following professionals worked on this program 1 December 1976-1 March 1977. The percentage of time worked is also shown.

Mr. P. L. Whelan	50%
Mr. R. A. Williamson	50%
Dr. G. L. Varnell	10%
Dr. J. L. Bartelt	Consultant
Dr. T. L. Brewer	Consultant
Dr. R. J. Dexter	Consultant
Dr. R. A. Robbins	Consultant
Mr. C. D. Winborn	Consultant

In addition, three technicians worked on the program.